AN2527
Application note

CLT3-4 termination in industrial automation logic inputs
STEVAL-IFP008V1

Introduction

The CLT3-4B (Current Limited Termination) is a quadruple logic input termination for sensor or mechanical switch interfaces. It is designed to work in 24 V_{DC} applications such as Programmable Logic Controller PLC, Programmable Automation Controller PAC, and Distributed I/Os systems used in factory automation.

The device optimizes the input V_I characteristic to reduce power dissipation. This becomes critical when the application cabinet or housing requires higher protection levels such as IP65 and IP67. These closed cabinets are used in various automated lines including the food and chemical industry. The power dissipated inside the module is very limited as there is usually no air circulation inside the box. The current limitation reduces the power losses in the sensor as well.

The most important challenge of CLT3-4 is the electrical protection and susceptibility it brings to the application. The CLT3-4B implements efficient protection diodes on each input and supply voltage lines. Associated serial resistors as described below ensure a higher level of susceptibility of the whole input module.

Thanks to its compact device package, the complete CLT3-4BT6 application occupies little space on the PCB compared to an equivalent discrete solution.

Features

- Termination for IEC61131-2 type 1 and 3 inputs
- 4 input channel topology
- Fully integrated internally fixed current limiter
- Optocoupler output drive
- Wide range supply voltage and temperature operation

Benefits

- Low power dissipation vs. discrete solution
- Few external components
- Over-voltage protection
- ESD according to IEC61000-4-2, Class 3, 8 kV air discharge, 6 kV contact discharge
- Excellent EMC robustness: voltage surge, fast transient burst immunity (±2 kV, ±4 kV)
- Compact module TSSOP20 package

General overview and device functionality can be found in document [1]. Document [2] describes typical applications and circuit behavior. This application note shows application modifications which improve the interface robustness and optimizes cost effectiveness. It also considers the connection of an indicator LED in series with the optocoupler. (According to IEC61131-2 each input high state should be indicated.) This connection reduces the number of components in the application bill of materials.

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1 CLT3-4BT6 description

The CLT3-4BT6 (Current Limited Termination) is a quadruple input digital termination device designed for 24 V_{DC} industrial automation applications. Typical applications are PLC (Programmable Logic Controller), PAC (Programmable Automation Controller), Distributed I/Os systems. It works as an interface for mechanical switches, relay contacts, two-wire or three-wire digital sensors (also known as proximity switches).

Available in a four-channel configuration, it offers a high-density termination by minimizing the external component count. It is housed in a TSSOP20 surface mount package to reduce the printed board size. Consisting of a parallel input voltage protection, a serial input-output current limiting circuit and an opto-coupler driver, each channel circuit terminates the connection between the logic input and the associated high side sensor or switch.

The CLT3-4BT6 device is used between the sensors and the opto-coupler of an input module. The current limiting circuit, connected between the input and the output pins, is compensated entirely over the temperature range. Furthermore, each channel runs independently of the others. Thanks to its low tolerance, the current limitation allows a drastic reduction of dissipation compared to a resistive input solution. The overall module requires less cooling capability and becomes smaller. Device functionality is visible in *Figure 1* and *2*.

Figure 1. CLT3 functionality principle - off state

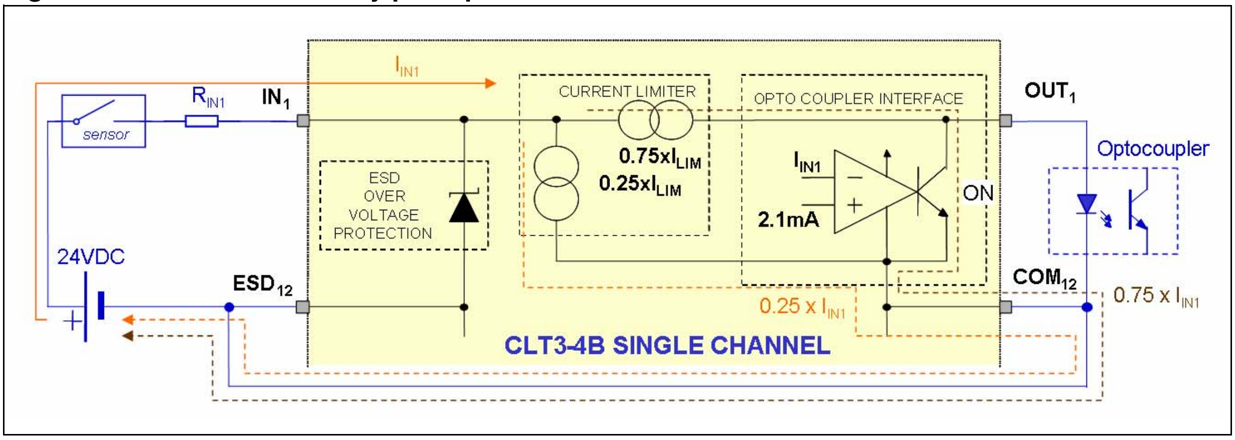
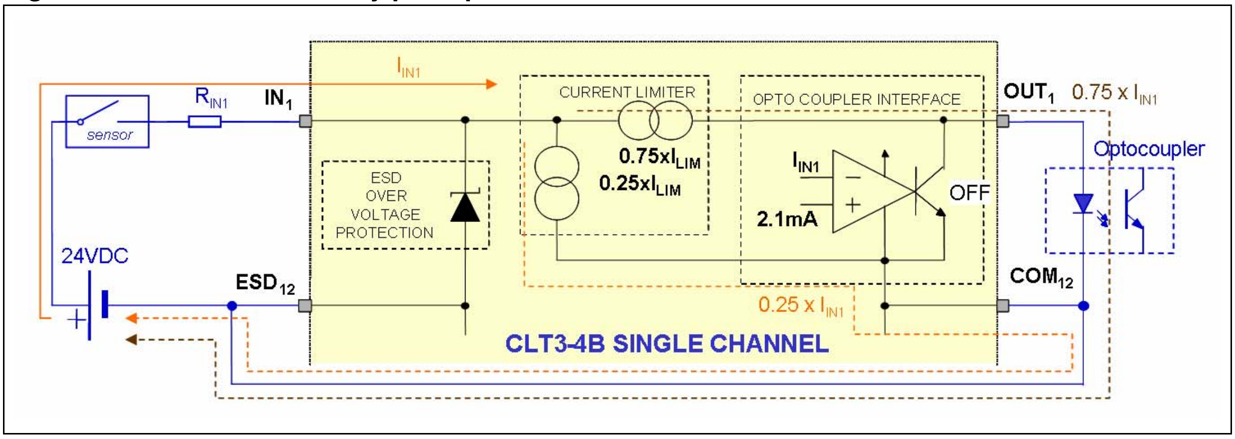


Figure 2. CLT3 functionality principle - on state



The application is connected with the sensor on the high-side (that is, to the power supply positive terminal). Each of the CLT3 channels uses an additional resistor connected in series with the sensor to take over a part of the total power dissipation. On the other hand it increases application robustness.

Each of the CLT3 inputs is protected by an integrated transient suppressor diode.

The current limiter sinks the current flowing through the sensor and resistor. The I_{LIM} value is typically 3 mA according to the datasheet. The input current (I_{IN1}) is then split into two portions. A quarter of this current always flows back to the power supply ground.

If the IIN1 current is lower than the comparator reference (2.1 mA typically), the comparator drives the output transistor so it shorts the appropriate current portion to the COM12 (GND) pin. It ensures the optocoupler is not powered.

When the I_{IN1} current rises above the comparator threshold, the transistor switches off. In this case the current can flow through the optocoupler.

Voltage threshold of the CLT3 is typically 3.4 V on the input pin which corresponds to 7.2 V on the application input considering the 1.8 kΩ serial resistor. The minimum output current, keeping the opto-coupler in on-state, is approximately 1.5 mA.

The CLT3-4BT6 protects the input module against transient electromagnetic interferences such as those described in the IEC61131-2 standard. The opto-coupler plays a role in the CLT3-4BT6 operation. The drop voltage of its input diode introduces a voltage offset in series with the CLT3-4BT6 channel. For efficient CLT3-4BT6 operation, this drop voltage should remain below 2 V (see CLT3-4BT6 datasheet for more details).

2 Demo board description

A representative application diagram is shown in *Figure 3*. This is the typical case often used in automated systems. It is compliant to type 1 and 3 input characteristics according to IEC61131-2 standard. The board can be supplied with voltage that ranges from 10 to 35 V_{DC} connected to the INPUT header J1 (pin 3 - positive, pin 4 - negative). The secondary supply voltage derives from the microcontroller or control logic supply voltage level. It is considered to be a 5 V_{DC} but the 3.0 V_{DC} or 3.3 V_{DC} are also applicable. The secondary supply voltage should be connected to the OUTPUT header (pin 3 - positive, pin 4 - negative).

Special attention should be given to the input resistors. Their type dramatically influences the application EMC - high voltage surge robustness (IEC61000-4-5). The resistors should sustain high peak voltage and current levels. A good example is the MELF MMB0207 from VISHAY. Peak ratings of such resistors are 70 W or 3 kV. The standard SMD 1206 resistors are not recommended as the rating is much lower, therefore the application fails at surge levels close to 1 kV (differential mode, 42 Ω/0.5 µF coupling).

The capacitors C1 to C4 work as noise filters.

A state-of-the-art optocoupler (TLP281-4) has been chosen mainly because of its cost effectiveness.

LED state indicators are connected on the secondary side. The energy which powers the LEDs on is taken from the logic power supply (Vapp). A different configuration is shown in *Section 6: Operation in type 1 mode with LED connected to CLT3-4 output*.

Reverse polarity protection against spurious reverse supply voltage connection is not required with CLT3. There is no issue with the reverse connection of the power supply to the board supply voltage lines since the serial resistor (Rc = 4.7 kΩ) limits the default current and CLT3 is designed to sustain negative bias of its substrate. With this application topology and 1.8 kΩ resistors on the inputs, the negative input has an off-state output while the others are still operative. The robustness of the input is secured by the resistor that should be rated to handle the reverse polarity dissipation (29^2 /1.8 kΩ = 0.47 W).

Figure 3. Application schematic diagram - basic configuration

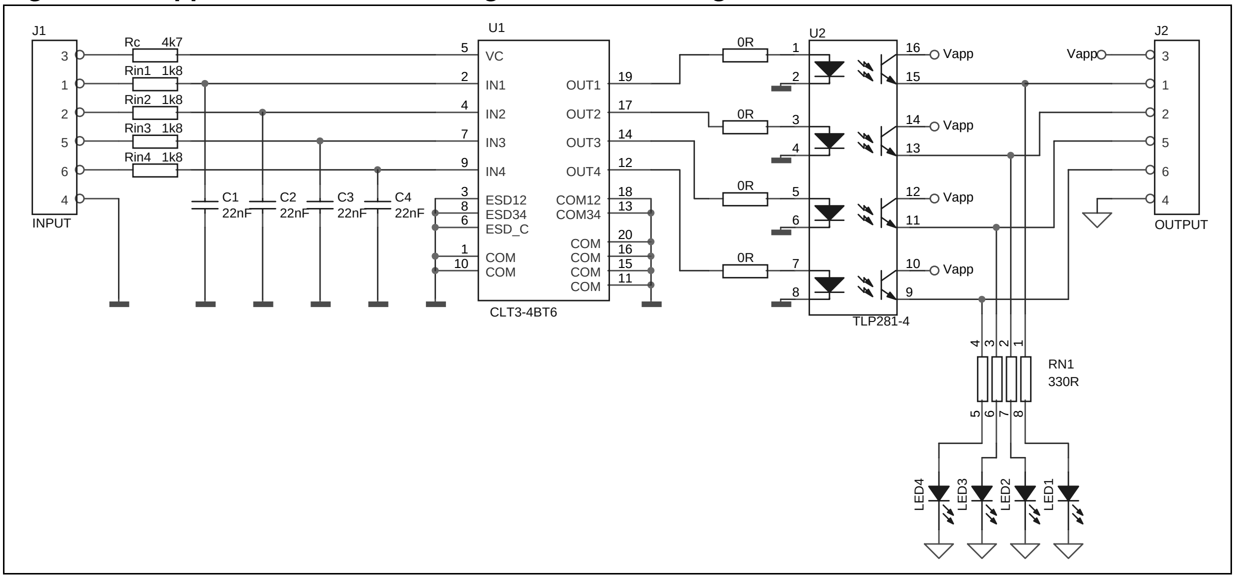


Figure 4. Signal conventions

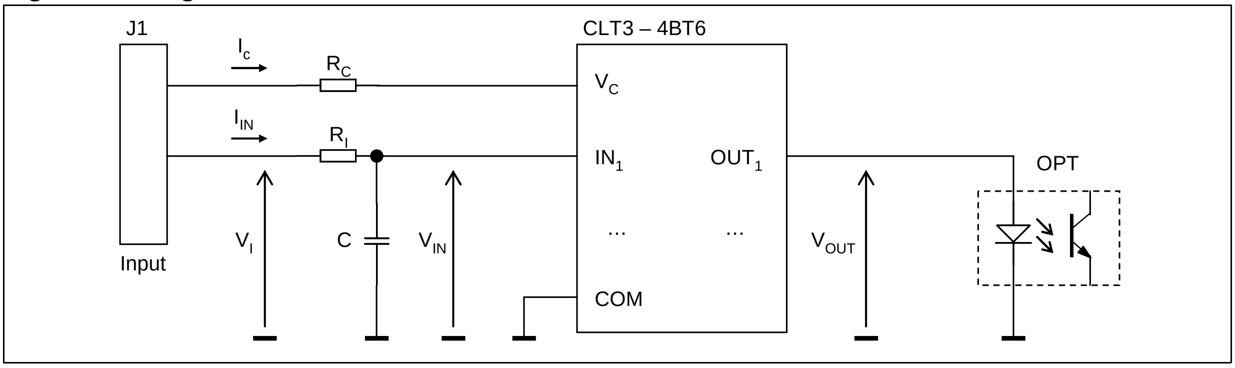


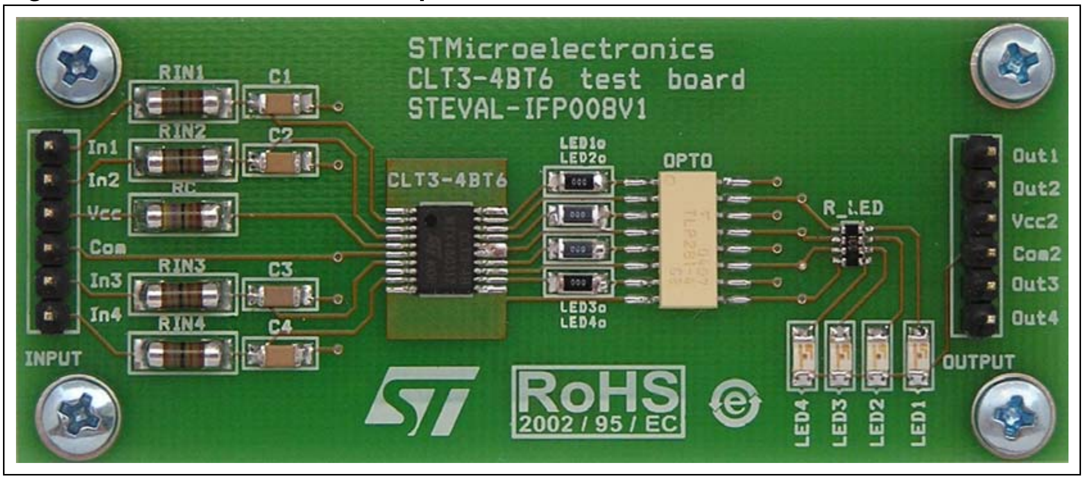
Table 1. Bill of material

ID	Reference	Value	Description	Package
1	C1, C2, C3, C4	22 nF/50 V	Ceramic capacitor X7R	SMD 1206
2	J1, J2	6 pin	Pin strip header 2.54 mm	SIP6
3	LED1, LED2, LED3, LED4		Green LED	SMD 1206
4	LED1o, LED2o, LED3o, LED4o		Optional: Green LED – low V_F	SMD 1206
5	Rin1, Rin2, Rin3, Rin4	1k8/300 V	Professional MELF resistors e.g. VISHAY - MMB0207	SMD
6	Rc	4k7/300 V	Professional MELF resistors e.g. VISHAY - MMB0207	SMD
7	RN1	330R	Resistor array	SMD 1206
8	U1	CLT3-4BT6	Current limited termination	TSSOP20
9	U2	TLP281-4	Optocoupler	SO16

Note: D 4: LED1o to LED4o: Optional. If assembled, the LEDs should be low forward voltage types.

Note: D 5 and 6: Rin, R_C are highly robust resistors for industrial use in order to achieve the high voltage surge level according to IEC61000-4-5.

Figure 5. Evaluation board - top view



3 Thermal management

The CLT3-4BT6 device limits the current that flows across each line. This causes an increase of the junction temperature. The maximal allowed junction temperature of the CLT3-4BT6 is 150°C. The TSSOP20 package has a thermal resistance specified in the datasheet. This parameter allows determining the maximal ambient temperature during the operation of the device. The ambient temperature to take into account is the air temperature close to the component.

The main equation corresponds to the following: $\Delta T_{j\text{-}a} = T_j - T_a = P_d\ R_{thj\text{-}a}$

Where:

- T_j: junction temperature,
- T_a: ambient temperature,
- P_d: power to dissipate,
- $R_{thj\text{-}a}$: junction to ambient thermal resistance.

This paragraph presents the method to evaluate the dissipated power and also the evolution of the R_{th} value versus the copper surface on the PCB.

The maximal ambient temperature determines the maximal allowed $\Delta T_{j\text{-}a}$. To estimate the maximal power dissipation, refer to the parameter of the datasheet that gives the maximal specification of the current limitation. The purpose is to add all "thermal supplies" inside the die. There are 3 main sources of the power dissipation: the 2 current limiters embedded in each line of the CLT device (see *Figure 5*), and the low current consumption of the V_C pin (I_C). Then, the maximal power dissipation can be estimated as follows:

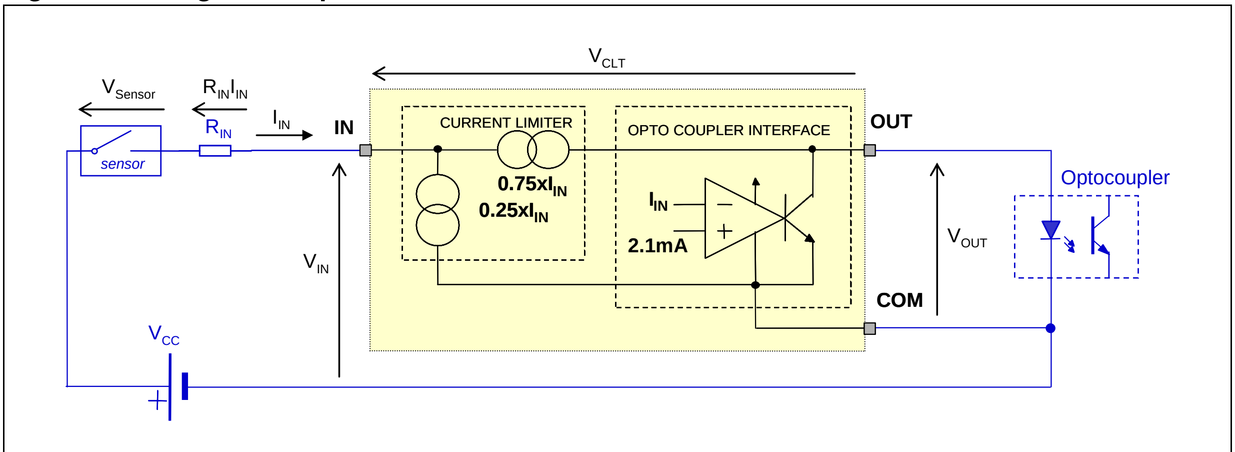
Equation 1

$$P = 4 \cdot [(V_{CLT} \cdot 0.75 \cdot I_{IN}) + (V_{IN} \cdot 0.25 \cdot I_{IN})] + V_C \cdot I_C$$

The worst case scenario occurs when I_{IN} and I_C are on the maximum limits. These maximal values are given in the datasheet:

- I_{IN} = 3.7 mA
- I_C = 800 µA

Figure 6. Single line equivalent circuit for thermal calculations



To calculate the drop voltage across the CLT device, the circuit of *Figure 3* gives the following equations:

Equation 2

$$V_{IN} = V_{CC} - V_{sensor} - R_{IN}I_{IN}$$

Equation 3

$$V_{CLT} = V_{IN} - V_{OUT}$$

The worst case scenario corresponds to the maximal supply voltage value (V_{CC}), and to the minimal drop voltage across the sensor (V_{SENSOR}) and across the diode of the opto-coupler (V_{OUT}).

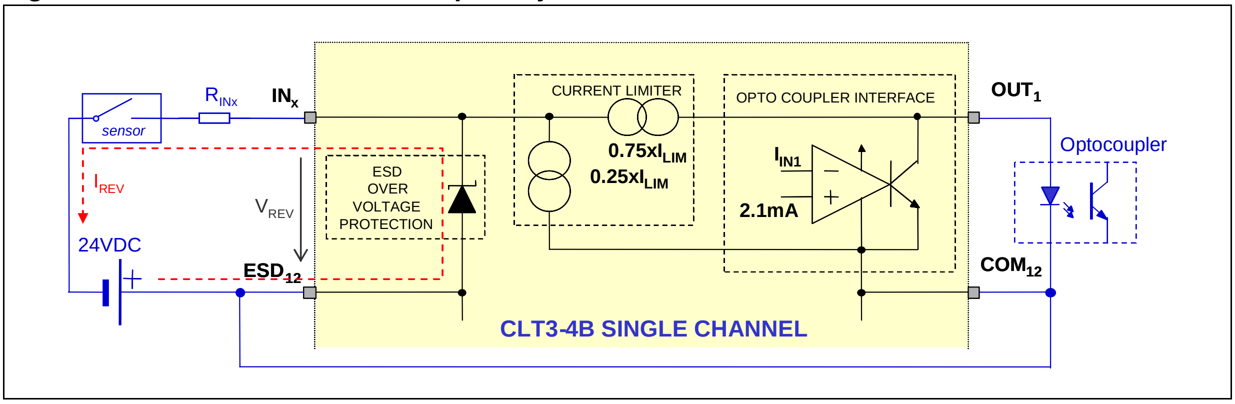
For example:

- V_{CC} = 30 V_{max}
- V_{SENSOR} = 0 V_{min}
- V_{OUT} = 0.7 V_{min}
- P_{TOTAL} = 360 mW

In the case of a maximal allowed ambient temperature equal to 100 °C, the thermal resistance must be lower than 139 °C/W. Since the maximal R_{th} value of the TSSOP20 package (0 cm²) is 120 °C/W, The CLT3-4 runs correctly at this ambient temperature.

In the final application we also have to consider other cases. One example is spurious connection of one channel to negative voltage. Circuit behavior of the one channel is visible in *Figure 7*.

Figure 7. One channel in reverse polarity



In this negative biasing of the input, the current (I_{REV}) flows through the protection diode. The voltage (V_{REV}) is then equal to the forward voltage of the protection diode and it is approximately 1 V at 20 mA.

All of the other inputs work in normal operation as visible in *Figure 2* or *Figure 5*.

The total power dissipation in this case can be calculated by the following formula:

Equation 4

$$I_{REV} = \frac{(V_{CC} - V_{REV})}{R_{IN}} = \frac{(30-1)}{1800} = 16.1\ \text{mA}; \quad I = \frac{(30-1)}{1800} = 16.1\ \text{mA}$$

Then

Equation 5

$$P = 3 \cdot [(V_{CLT} \cdot 0.75 \cdot I_{IN}) + (V_{IN} \cdot 0.25 \cdot I_{IN})] + V_C \cdot I_C + V_{REV} \cdot I_{REV} = 290 \text{ mW}$$

If we consider the same condition as above - maximum ambient temperature of 100 °C, we need to achieve the thermal resistance of 179 °C/W. The CLT3 works correctly without additional heatsink. Connecting the input in reverse polarity condition, the total power dissipation decreases. It allows biasing all of the CLT3 inputs by reverse polarity current without taking any risk of component damage.

Special care must be taken on the serial resistors rating. During normal operation under worst case conditions, the power ratings of the serial resistors are:

- 25 mW for the input serial resistors (R_{IN}),
- 3 mW for the supply serial resistor (R_C).

During the reverse polarity connection at 25°C, the resistors must be able to dissipate:

- 470 mW - the input serial resistors (R_{IN}),
- 190 mW - the supply serial resistor (R_C).

4 EMC requirements

4.1 Description of the procedure to evaluate the robustness of the CLT3-4BT6

The reference to evaluate the robustness of the CLT3-4BT6 product is the IEC61131-2 international standard. This international standard gives all requirements and conditions of tests that must be performed on the programmable logic controllers (PLC) and their associated peripherals.

This document focuses on the most stressful tests for the CLT3-4BT6 product. The immunity of the CLT3-4BT6 is tested according to the standards.

The IEC61131-2 standard specifies the Electromagnetic Compatibility (EMC) requirements and the nature of the tests to perform in order to determine if the system meets these requirements (paragraph 7: "EMC requirements" and paragraph 8: "EMC type tests and verifications" of the Ed2 of the standard). The levels of each test depend on the zone where the system will be installed. The most typical industrial environmental levels correspond to zone B: local power distribution zone and dedicated power distribution zone (see table 28: “EMC immunity zones“ of the IEC61131-2-Ed2 standard). The following paragraphs recall the test levels for this zone.

4.2 ESD tests (according to the IEC61000-4-2)

The electrostatic discharge test shall be applied to operator accessible devices. This means that these tests have to be performed on each connector pin. The required levels are: air discharge: +/-8 kV contact discharge: +/-6 kV.

The PLC system shall continue to operate as intended. Temporary degradation of the performance is acceptable during the test, but the system must recover by itself after the test (B criterion according to the IEC61131-2 standard).

4.3 Burst tests (according to the IEC61000-4-4)

The fast transient burst tests must be applied on all the input pins of the system. A capacitive clamp-coupling device (50-200 pF) must be used as described in the IEC61000-4-4 standard. The required burst voltage levels are: analog or dc I/O: +/-1 kV, dc power line: +/-2 kV. The PLC system shall continue to operate as intended. Temporary degradation of the performance is acceptable during the test, but the system must recover by itself after the test (B criterion according to the IEC61131-2 standard).

4.4 Surge test (according to the IEC61000-4-5)

Since the voltage surge consists of a single but energetic pulse, the CLT3-4BT6 device embeds an over-voltage protection on each point. The absorbed energy complies minimally with the requirements of the IEC61131-2 standard. The high energy surge test must be applied on all input pins of the system. For all analog inputs, the coupling method is a 42 Ω serial resistance and a 0.5 µF capacitor. For dc power line, the coupling is 2 Ω, 18 µF with differential mode, and 12 Ω, 9 µF with common mode. The required voltage surge levels are: analog or dc I/O: 0.5 kV (line-to-line and line-to-earth coupling modes), dc power line: 0.5 kV (line to line), dc power line: 1 kV (line to earth). The PLC system shall continue to operate as intended. Temporary disruption of the operation is acceptable during the test, but the system must recover by itself after the test (B criterion according to the IEC61131-2 standard).

4.5 Conducted disturbance tests (according to the IEC61000-4-6)

The conducted radio frequency interference test must be applied on all input pins of the system. The frequency range is 150 kHz to 80 MHz, with a 80% amplitude modulation by a 1 kHz sinusoidal wave. A CDN (Coupling Device Network) or a current coupling clamp (as described in the IEC61000-4-6 standard) has to be used to apply stress to the system. The required level is: 3 V_{RMS}, whatever the tested system input is. The PLC system shall continue to operate as intended. No loss of function or performance is acceptable ("A" criterion according to the IEC61131-2 standard).

4.6 Reverse analog input polarity tests

The test procedure is described by the IEC61131-2 standard (paragraph 5.4.4.5 of the Ed2 of the standard). A signal of reverse polarity (negative voltage) for unipolar analog inputs is applied for 10s. The result of this test shall be as stated by the manufacturer. Each input of the CLT3-4BT6 device may be biased to a reverse polarity. This case corresponds to a connection mistake, or a reverse biasing that is generated by the demagnetization of a monitored inductive solenoid. The involved input withstands the high reverse current up to 20 mA; its opto-coupler is off and protected by the conducting input diode. The other inputs remain operational. Considering the supply operation the serial resistor limits the reverse current.

5 EMC testing

The EMC requirements according to IEC61131-2 have been verified. Application tests show better voltage surge robustness (IEC61000-4-5) keeping the other results on the same level (compared to AN1608). The application passed the 2 kV surge level with test criteria B which means temporary disruption. It is the best achievable criteria. The input lines have been coupled to the generator through 0.5 µF - 42 Ω, supply voltage line through 18 µF - 2 Ω in differential mode, 9 µF - 12 Ω in common mode. Test requirements and results are listed in the table below. No additional protection devices have been used in the application. In most EMC test cases, the CLT3-4 allows the standard to meet with a factor two on performance results.

Table 2. EMC Immunity test requirements & results

	Minimum requirements of international standards			Robustness of the CLT3-4BT6 demoboard			
	Tests conditions		**Levels**	**Tests conditions**		**Levels**	**Behavior of the CLT**
ESD test IEC61000-4-2	Air discharge		±8 kV	R_C=4.7 kΩ R_{IN}=1.8 kΩ		±8 kV	
	Contact discharge		±4 kV	R_C=4.7 kΩ R_{IN}=1.8 kΩ		±6 kV	
Burst test IEC61000-4-4	Analog input		±1 kV	R_{IN}=1.8 kΩ	C=22 nF	±4 kV	No failure, no disturbance
	DC power line		±2 kV	R_C=4.7 kΩ			
Surge test IEC61000-4-5	Analog input	42 Ω, 0.5 µF differential and common mode	±0.5 kV	Analog input	R_{IN}=1.8 kΩ	±2 kV	No failure, temporary disturbance
	DC power line	2 Ω, 18 µF differential mode	±0.5 kV	DC power line	R_C=4.7 kΩ	±2 kV	
		12 Ω, 9 µF common mode	±1 kV			±2 kV	
Conducted disturbance test IEC61000-4-6	150 kHz to 80 MHz		$3V_{RMS}$	150 kHz to 80 MHz	RIN=1.8 kΩ C=22 nF at the INPUT	$10V_{RMS}$ AM ± 80%	No failure, no disturbance
Reverse input polarity test	$-V_{CC}$ applied to one input during 10s			$-30V_{DC}$ applied to one input, $+30V_{DC}$ on the others			No failure, no cross talk

6 Operation in type 1 mode with LED connected to CLT3-4 output

The application board has several possibilities for the connection of indication LEDs. The normal configuration as described above uses the indication LEDs connected to the secondary side - supplied from the Vapp supply voltage.

The LEDs can be also connected in series with the optocouplers. This can be achieved by replacing the zero-Ω 1206 junctions by the LEDs - "LED1o to LED4o" pcb assembly positions.

When the LEDs are connected to the CLT3 output in series with the optocoupler, the functionality is limited to the digital input type 1 according to IEC61131-2. The total forward voltage which equals the LED plus optocoupler forward voltages ($V_F = V_{FLED} + V_{FOPT}$) is the key parameter that influences CLT3 behavior. To achieve the highest margin in the VI characteristic according to ON, OFF and Transition regions definition in the IEC61131-2, the total V_F should be minimized. If type 3 compliancy is requested, the LEDs connected in series with the optocoupler should be replaced by zero-Ω 1206 junctions.

The OFF threshold is strongly influenced by the total voltage drop V_F. For type 3 compliance the V_F should be kept approximately below 2 V according to [1]. In the case of digital input type 1 application, the limit is higher - approximately 2.9 V at 25 °C. Anyway the datasheet [1] restricts the maximum allowed steady state output voltage to 2.5 V which the application should ensure. The total V_F usually varies over the temperature range. It rises when the temperature decreases. Therefore the application behavior should be checked at the low limit of the ambient temperature. It is not recommended to use this configuration for temperatures lower than -15 °C.

Figure 8. Application schematic diagram - LEDs in series with optocoupler

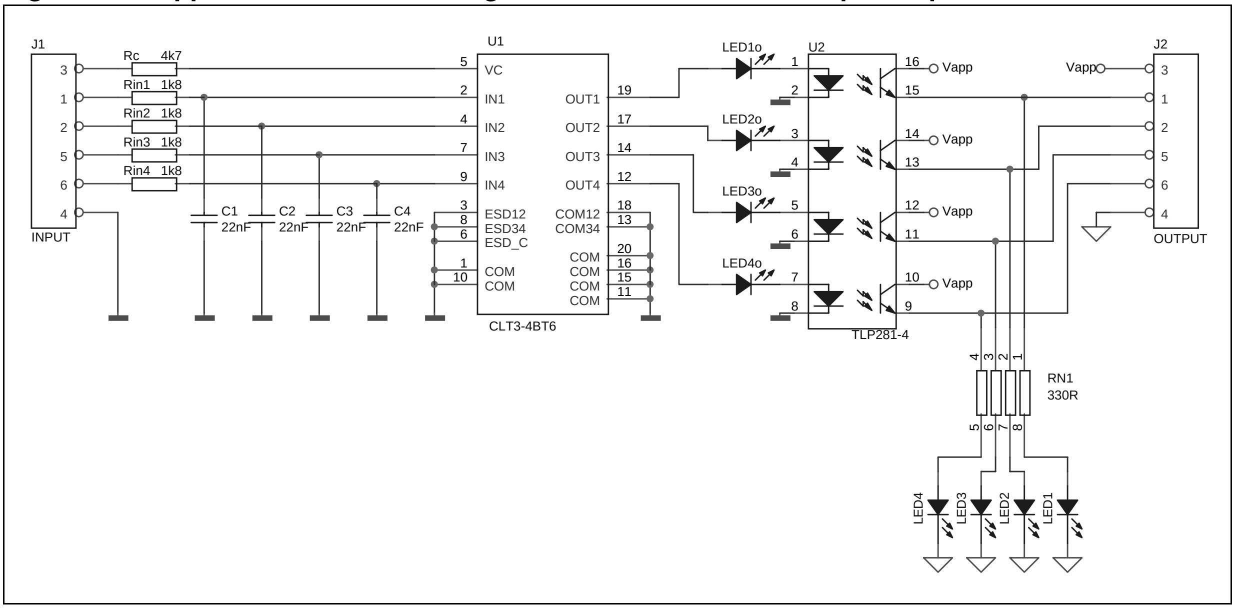


Figure 9. Measurement V_F = 2.7 V at 25 °C

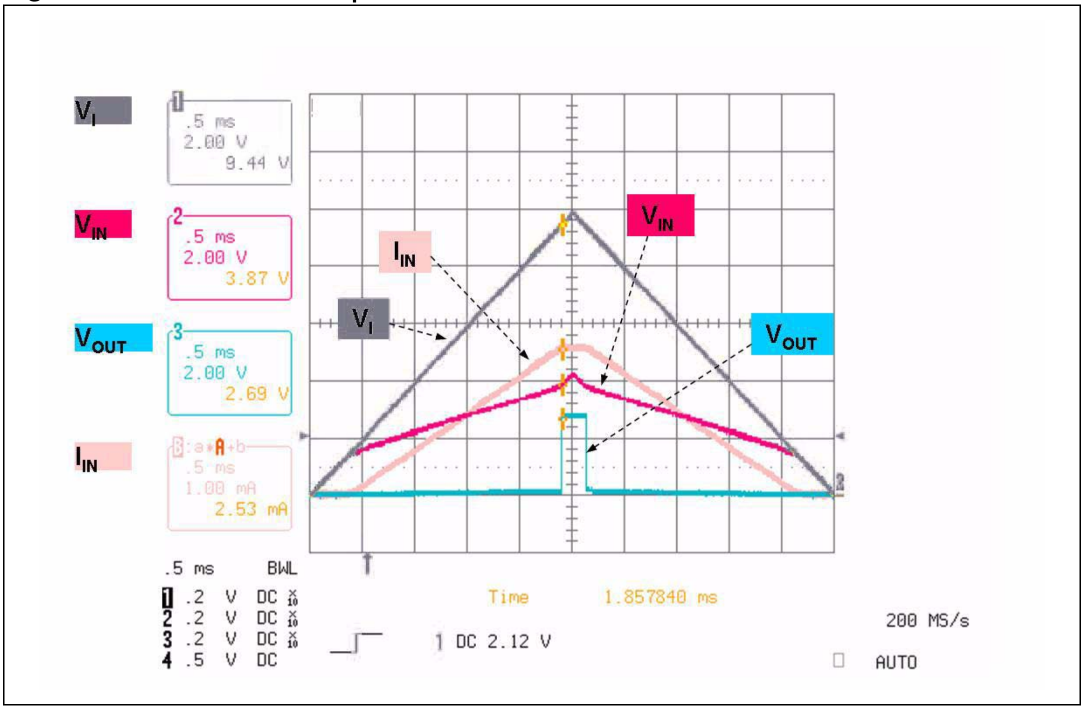


Figure 10. Measurement V_F = 2.9 V at 25 °C

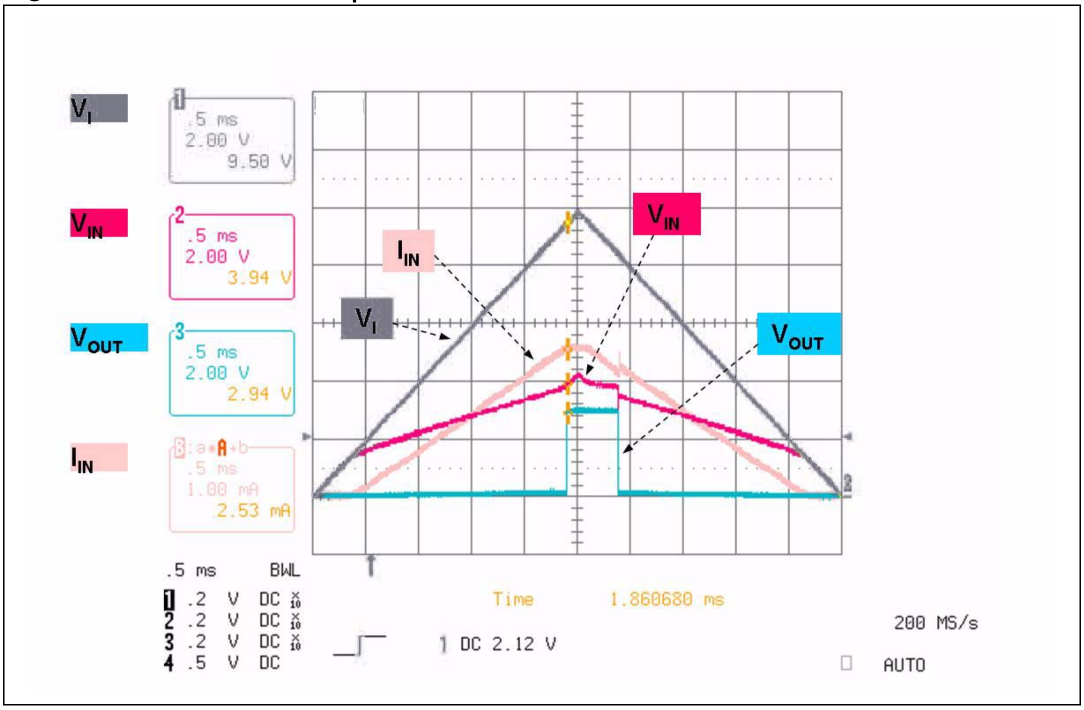


Figure 11. Measurement V_F = 3.1 V at -15 °C

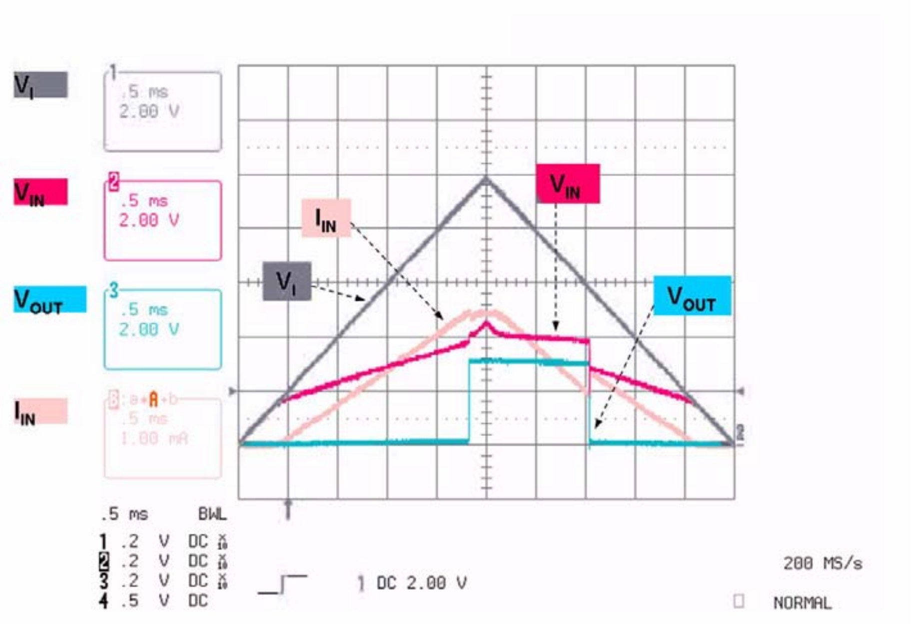


Figure 12. Measurement V_F = 3.2 V at -25 °C

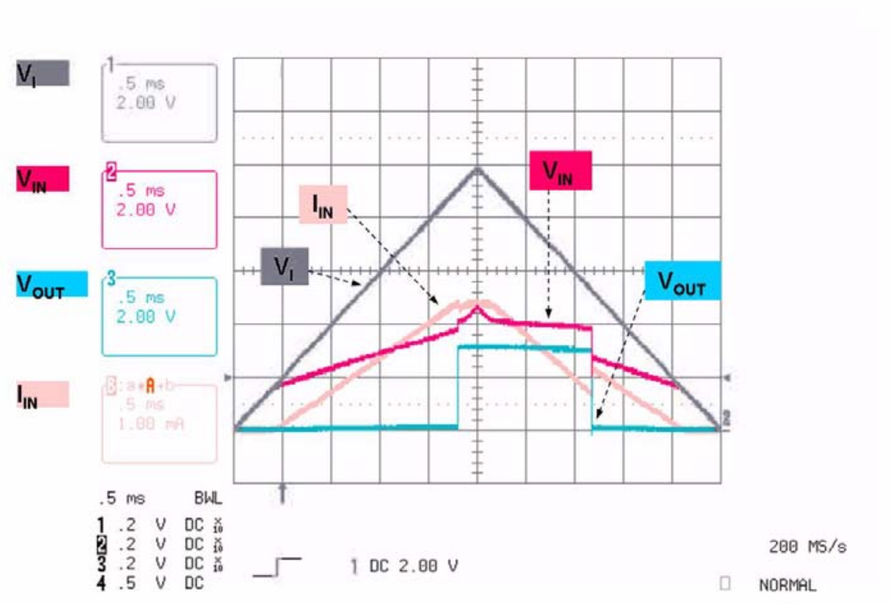


Figure 9 shows the application channel testing with a red LED which has the lowest forward voltage, V_{FLED} = 1.7 V, V_{FOPT} = 1 V, $V_F = V_{FLED} + V_{FOPT}$ = 1.7 + 1 = 2.7 V at 25 °C. All of the other figures consider usage of a green LED with V_F approximately 1.9 V at 25 °C. V_{IN}, I_{IN} discontinuity at switch off phase starts to be visible.

When the temperature decreases to -15 °C, V_F rises approximately to 3.1 V and the type 3 compatibility is lost as shown in *Figure 11*. The CLT output is still ON (V_{OUT}) but the input current (I_{IN}) decreases below the 1.5 mA limit (OFF region limit according to IEC61131-2).

Further decrease of the temperature to -25 °C is visible in *Figure 12*. The interface is still type 1 compatible but the margin is small. According to IEC61131-2 input type 1 transition region definition: V_I, I_{IN} on the falling edge of the V_{OUT} should be higher than 5 V, 0.5 mA. *Figure 12* shows approximately 5.2 V, 0.6 mA.

7 Conclusion

This document shows that the CLT3-4 application works in a harsh environment without any problems. The industrial standard requirements are fulfilled. Moreover the test levels are higher and twice than the requested levels for most of the final products. No additional protection devices are necessary to use, which has a positive influence on the application cost effectiveness. The new proposed application diagram allows any reverse polarity negative effects to be eliminated, the internal dissipation to be reduced (<0.36 W) and the input resistor to be kept to a reasonable level (< 0.5 W). The CLT3 application passed the reverse polarity tests including the thermal management considerations. An application modification with LED indicators in series with optocouplers is proposed for input Type1 applications, usage of low-forward voltage components and lower temperature limit to approximately -15 °C.

8 References

1. CLT3-4BT6 device datasheet
2. CLT3-4BT6 demoboard: check the robustness of CLT3-4BT6 application note
3. EC61131-2 - programmable controllers - equipment requirements and tests
4. EN60947-5-2: "low-voltage switchgear and controlgear - Part 5-2: Control circuit devices and switching elements - proximity switches"
5. EC61000-4-2: "electrostatic discharge"
6. EC61000-4-4: "electrical fast transient/burst immunity test"
7. EC61000-4-5: "surge immunity test"
8. EC61000-4-6: "immunity to conducted disturbances, induced by radio-frequency fields"

9 Revision history

Table 3. Document revision history

Date	Revision	Changes
15-May-2007	1	First issue
26-Sep-2007	2	– Title changed from “CLT3-4B application tips” to “CLT3-4 termination in industrial automation logic inputs STEVAL-IFP008V1” – Minor text changes – Added *Figure 1*, *2*, *5*, *6*, *7* – Modified *Figure 3*, *4*, *8* – Added *Table 2*